"Express Mail" mailing label number EL443496680US

APPLICATION FOR LETTERS PATENT
OF THE UNITED STATES

NAME OF INVENTORS:

Hartmund TERLETZKI
27 Skidmore Road
Pleasant Valley, NY 12569

Germany

Gerd FRANKOWSKY
Vogelbeerstr. 11
82024 Munich, Germany

Germany

TITLE OF INVENTION: LEVEL-SHIFTING CIRCUITRY HAVING "HIGH" OUTPUT IMPEDANCE DURING DISABLE MODE

TO WHOM IT MAY CONCERN, THE FOLLOWING IS
A SPECIFICATION OF THE AFORESAID INVENTION

Express Mail Label No.: EL443496680US

LEVEL-SHIFTING CIRCUITRY HAVING "HIGH" OUTPUT IMPEDANCE DURING DISABLE MODE

BACKGROUND OF THE INVENTION

This invention relates generally to level-shifting circuitry.

As is known in the art, level-shifting circuitry is used to shift lower voltage signal levels to higher voltage signal levels. One example of such circuit is shown in FIG. 1. Such circuit 9 is formed on a semiconductor chip and includes a pair of N type Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) N_1 and N_2 and a pair of P type MOSFETs P_1 P_2 arranged as shown. The P type MOSFETs have the bulk silicon connected to an external +2.5 volt power source. The N type MOSFETs have the bulk silicon connected to ground. The N type MOSFET N_1 is a low threshold voltage transistor. The gate of transistor N_1 is connected to an internal +2.1 volt source. The input voltage (IN) is a logic signal having logic 1, here represented by +2.1 volts or a logic 0 state, here represented by ground potential. Here, the level-shifter also provides an inversion in the logic state of the input signal as well as shifting the input signal logic 1 state from +2.1 volts to a higher voltage output signal logic 1 state, here +2.5 volts. Thus, in operation, when the input voltage is logic 0, transistors N_1, and P_2 are "on" and transistors P_1 and N_2 are "off", thereby providing a logic 1, here a +2.5 volt level, at the output OUT. Thus, the input logic 1 condition of a +2.1 volt input signal has been shifted to a +2.5 volt output logic 1. On the other hand, when the input voltage IN is logic 1 (i.e., here +2.1 volts), transistors N_1, and P_2 are "off" and transistors P_1 and N_2 are "on", thereby providing ground potential (i.e., an output logic 0) at the output OUT.

SUMMARY OF THE INVENTION

In accordance with the present invention, level-shifting circuitry is provided having a level-shifting section responsive to an input logic signal. The input logic signal has a first voltage level representative of a first logic state or a second voltage level representative of a second logic state. The level-shifting section provides an output logic signal at an output terminal having a third voltage level representative of the first logic

state of the input logic signal. The level-shifting circuitry also includes an enable/disable section responsive to an enable/disable signal for placing the output terminal at a relatively high output impedance condition independent of the logic state of the input signal during a disable mode.

In one embodiment, the level-shifting section includes: an input transistor having a control electrode, a first electrode coupled to the input logic signal, and a second electrode. An output pair of serially coupled complementary type transistors is provided. A first one of the pair of transistors has a first electrode coupled to a source of the third voltage level through a first switching transistor and a control electrode coupled to the second electrode of the input transistor. (It should be noted that in the case of a FET, the terms first and second electrode refer to source and drain electrodes, it being understood that while each transistor has a source and drain electrode, the terms may be used interchangeable. Further, in the case of a FET, the term control electrode refers to the gate electrode). A junction between the output pair of transistors provides an output terminal for the level-shifting circuitry. The junction provides the output terminal. A control electrode of the second one of the pair of transistors is connected to the first electrode of the input transistor. The second one of the pair of transistors has a second electrode coupled to the second voltage level through a second switching transistor. The first and second switching transistors are fed by the enable/disable signal.

In one embodiment, the level-shifting section includes an additional transistor. The additional transistor has a control electrode connected to the junction, a first electrode coupled to the source of the third voltage level through the first switching transistor and a second electrode connected to the second electrode of the input transistor. In one embodiment, the input transistor and the additional transistor are of opposite conductivity type.

In one embodiment, the enable/disable circuit includes an inverter fed by the enable/disable signal, such inverter having an output coupled to the control electrode of the first switching transistor.

In one embodiment, the inverter is powered by a source of the first voltage level and the enable/disable signal operates between the first and second voltages. In such

embodiment, the inverter comprises a level shifter for shifting the level of the enable/disable signal from the first voltage level to the third voltage level and for feeding such third voltage level to the control electrode of the first switching transistor to placing the first switching transistor to a non-conducting condition during the disable mode.

The details of one or more embodiments of the invention are set forth in the accompanying drawings and the description below. Other features, objects, and advantages of the invention will be apparent from the description and drawings, and from the claims.

DESCRIPTION OF DRAWINGS

FIG. 1 is a schematic diagram of a level-shifting circuit according to the PRIOR ART;

FIG. 2 is a. schematic diagram of a level-shifting circuit according to the invention; and

FIG. 3 is a. schematic diagram of a level-shifting circuit according to the invention.

Like reference symbols in the various drawings indicate like elements.

DETAILED DESCRIPTION

Referring now to FIG. 2, level-shifting circuitry 10 is shown to include: a level-shifting section 12 responsive to an input logic signal IN and an enable/disable section 14 fed by an enable/disable signal ENABLE. The input logic signal IN has a first voltage level, here +2.1 volts representative of a first input logic state, here logic 1, and a second voltage level, here ground, representative of a second input logic state, here logic 0.

The level-shifting section 10 provides an output logic signal at output terminal OUT. The output logic signal at the output terminal OUT has a third voltage level, here +2.5 volts representative of the first output logic state, here logic 1, or the second voltage level, here ground, representative of the second output logic state, here logic 0. Here, during the enable mode (to be described hereinafter), in response to the input logic signal IN having an input logic 1 state (i.e., +2.1 volts), the output logic signal at output

terminal OUT will be the ground thereby representing an output logic 0 state. On the other hand, during the enable mode, in response to the input logic signal IN having an input logic 0 state, here ground, the output logic signal at the output terminal OUT will be the third voltage level +2.5 volts thereby representing an output logic 1 state. During a disable mode, the enable/disable section 14 places the output terminal OUT at a relatively high impedance condition independent of the logic state of the input logic signal IN. By high impedance it is meant that the substantially little, or no current, passes though the output terminal OUT.

More particularly, the level-shifting section 12 includes an input transistor N_1 having a control, here gate, electrode coupled to a +2.1 volt supply, a first electrode coupled to the input logic signal IN, and a second electrode. An output pair of serially coupled complementary type transistors, i.e., P type MOSFET P_2 and N type MOSFET N_2, is provided. A first one of the pair of transistors P_2 has a first electrode coupled to a source, not shown, of the third voltage level (+2.5 volts) through a first switching transistor P type MOSFET P_3 and a control electrode coupled to the second electrode of the input transistor N_1. A junction 16 between the output pair of transistors P_2, N_2 provides the output terminal OUT for the level-shifting circuitry 10. A control electrode of the second one of the pair of transistors N_2 is connected to the first electrode of the input transistor N_1. The second one of the pair of transistors N_2 has a second electrode coupled to the second voltage level, here ground, through a second switching transistor N_3. The first and second switching transistors P-type MOSFET P3 and Ntype MOSFETs N3 are fed by the enable/disable signal ENABLE, the transitor P_3 beinbg coupled to the enable/disable signal ENABLE via an inverter 18, as shown. The level-shifting section 12 includes an additional transistor P type MOSFET P_1. The additional transistor P_1 has a control electrode connected to the junction 16, a first electrode coupled to the source of the third voltage level +2.5 through the first switching transistor P_3 and a second electrode connected to the second electrode of the input transistor N_1. The input transistor N_1 and the additional transistor P_1 are of opposite conductivity type. The enable/disable circuit 14 includes an inverter 18 fed by the enable/disable signal ENABLE. The inverter 18 having an output coupled to the control electrode of the first switching transistor P_3.

Sub a'

The inverter 18 is powered by a source, not shown, of the third voltage level, +2.5 volts. The control electrode of the input transistor N_1 is coupled to the source of the first voltage level +2.1.

In operation, during the disable mode, the enable/disable signal ENABLE is logic 0, here a voltage at ground. In the disable mode, the output of the inverter 18 is at the third voltage i.e., +2.5 volts. Such +2.5 volts turns transistors P_3 and N_3 "off" thereby placing the output terminal OUT in a high impedance condition independent of the logic state of the input logic signal IN.

During the enable mode, the enable/disable signal ENABLE is logic 1, here the third voltage level, +2.5 volts. The output of inverter 18 is at ground. Thus, transistors N_3 and P_3 are "on" independent of the logic state of the input logic signal IN. In such condition, in response to the input logic signal IN having an input logic 0 state, here ground, the output logic signal at the output terminal OUT will be +2.5 volts thereby representing output logic 1 state.

More particularly, in the enable mode, the enable/disable signal ENABLE is a logic 1, here the third voltage level, +2.5 volts. In such enable mode, if the input logic signal IN is a logic 0, here ground, transistors $N_1$and P_2 and turn "on" and transistors N_2 and P_1 turn "off" thereby producing the third voltage level, +2.5 volts, at the junction 16. The third voltage level (+2.5 volts), here output logic 1, is coupled to the output terminal OUT because transistor N_2 is "off". On the other hand, if during the enable mode the input logic signal IN is logic 1, here +2.1 volts, transistors N_1, P_2 turn "off" while transistors N_2 and P_1 turn "on" thereby driving junction 16 to ground. This ground, i.e., output logic 0 state appears at the output terminal OUT because transistor P_2 is "off".

It is noted that the operation described above, the inverter 18 is powered by the source of the third voltage level +2.5 volts and thus, the enable/disable signal ENABLE must be at +2.5 volts during the enable mode. Here, the source of the +2.5 volts is an external voltage source. In some applications it might be desirable to use the internal source of the first voltage level, +2.1 volts for generating the enable mode condition of the enable/disable signal ENABLE. In such application, an alternative level-shifting circuitry is shown in FIG.3.

Thus, referring to FIG. 3, the level-shifting circuitry 10' is shown where the inverter 18 of FIG. 2 is replaced with an inverter which also provides level-shifting. More particularly, the inverter 18 of FIG. 2 is provided by the level-shifting circuitry 9 described above in connection with FIG. 1. The inverter/level shifter 9 includes a level shifter thus shifts the level of the enable/disable signal ENABLE from the first voltage level +2.1 to the third voltage level +2.5 and feeds such third voltage level +2.5 to the control electrode of the first switching transistor P_3 to placing the first switching transistor P_3 to a non-conducting (i.e., "off") condition during the disable mode. More particularly, the inverter/level-shifter 9 is here the level-shifting circuitry 9 shown and described above in connection with FIG. 1, here however, the level-shifting circuitry of FIG, 1 is fed by the enable/disable signal ENABLE and not the input logic signal IN, as in FIG. 1. Thus, in the disable mode, here again the output terminal is at a high output impedance independent of the logic state of the input logic signal IN.

A number of embodiments of the invention have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the invention. Accordingly, other embodiments are within the scope of the following claims.